REMARKS

The allowance of Claims 19 -- 23 is noted with appreciation.

The remaining independent claims as well as a number of dependent claims have been amended to better define the invention, and several dependent claims have been amended for consistency with the claims from which they depend.

In view of these amendments and for the reasons set forth below, it is respectfully submitted that the various rejections have been overcome and that this application is in condition for allowance. Accordingly, favorable reconsideration of this application is respectfully requested.

The Rejection Under 35 U.S.C. §112

The rejection of Claims 34 - 35 under 35 USC §112 is traversed. Claim 34 is directed to a set of software instructions stored on at least one medium, the instructions being executable on a processor for performing the recited operations, which correspond generally to the method set forth in Claim 12. Claim 34 has been amended to improve its form and to clarify that these operations are a method.

Claim 34 explicitly recites that the set of software instructions are stored on at least one medium in the storage switch. Accordingly, the claim is clear on its face that there is at least one medium, and that there may be more than one medium for storing instructions. It is respectfully submitted that the claim satisfies the requirements of Section 112, second paragraph. As to the Examiner's statement that the "claim" does not provide support for the medium, it is respectfully pointed out that this is not the function of a claim, but rather it is the specification which must provide support for a

claim element under Section 112. To the extent that the Examiner intended to refer to any absence of explicit support in the specification for the "medium", the specification has been amended at paragraph [0087] to provide explicit support for this element. (It is noted that Claim 34 was an original claim and, therefore, part of the original disclosure.)

In view of these amendments, it is submitted that the rejections under Section 112 are overcome.

The Rejections Under 35 U.S.C. §101

As noted, Claim 34 has been amended to clarify that it is directed to a set of instructions executable by a processor for performing a method comprising a series of operations set forth in the claim. As such, the claim is not claiming "instructions", but rather is directed to a medium (an article of manufacture) containing software instructions, and is in the form of a classic Beauregard-type claim that was explicitly approved by the Commissioner. See *In re Beauregard*, 53 F.3d 1583, 35 USPQ 2d 1383 (Fed. Cir. 1995).

Accordingly, it is respectfully submitted that Claim 34 is directed to statutory subject matter, and that this rejection is overcome.

The Rejections Under 35 U.S.C. §103

The claimed invention is concerned with virtualization of storage packets by a storage switch which routes the packets between servers and physical storage targets in a storage network. The packets arrive at a storage switch destined for a virtual storage target that is provisioned on one or more physical storage targets. The virtual

storage target is designated by a virtual target address in the packet, and virtualization comprises translating the virtual target address in the packet to a physical target address of a physical storage device on which the virtual storage target is provisioned. This address translation process (virtualization) is performed by the storage switch without buffering the packet, or at line speed. The claims are directed to methods, storage switches or linecards for performing the virtualization process of the invention. The independent claims, except for independent Claim 19 which was allowed, have been amended to clarify and better define the invention.

The rejections of the claims under 35 USC §103 on various combinations of U.S. Patent No. 6,880,070 to Gentieu et al., published application U.S. 2005/0111364 to Hipp, U.S. Patent No. 5, 524,254 to Morgan et al., U.S. Patent No. 6,693,906 to Tzeng and U.S. Patent No. 6,400,730 to Latif are respectfully traversed. For the reasons set out below, it is respectfully submitted that none of the various prior art references of record individually or in combination teaches or suggests the invention set out in the independent claims, and cannot render any of the independent claims unpatentable under 35 USC §103. Moreover, it is further respectfully submitted that the prior art references cannot be combined in the manner suggested by the office in the rejections, and that no logical combination of the references would produce the claimed invention, absent impermissible modification and reconstruction of both the structure and the functioning of the references, contrary to *KSR v. Teleflex, infra*.

Accordingly, the rejections of the claims under 35 USC §103 on various combinations are traversed, and it is submitted that these rejections should be withdrawn.

Claims 1, 2, 7 and 9

The rejection of Claims 1, 2, 7 and 9, comprising independent Claims 1 and 9, on Gentieu in view of Hipp is traversed.

Claim 1, as amended, is directed to a method for routing packets between servers and physical storage targets by a storage switch in a storage network. The claim recites, in relevant part:

> (a) receiving at a first port of the switch a packet that specifies as a destination a virtual storage target provisioned on a physical storage target;
>
> (b) sending at a second port of the switch the packet to said physical storage target; and
>
> wherein said sending comprises virtualizing said packet by translating a first address of said virtual storage target to a second address of said physical storage target without buffering the packet.

Claim 9 is similar except that it recites that the virtualizing occurs at wire speed rather than without buffering the packet.

Contrary to the Office's assertion, Gentieu does not disclose or suggest address translation in a storage network without buffering packets, or at wire speed, as claimed. Gentieu discloses a synchronous pipeline protocol processor in a communications network for converting different data traffic protocols to a common protocol. Gentieu's pipeline processor operates on serial data streams that are shifted serially into the pipeline processor to convert between data protocols, in contrast to conventional microprocessors where data is required to be moved in or out of registers

or internal memory and where the instructions clock are not synchronous with the I/O clock. (See col.. 4, lns 18-28.) Gentieu discloses nothing about translating an address in a packet of a virtual storage target to the address of a physical target on which the virtual target is provisioned, as claimed, and does not disclose or suggest address translation without buffering the packet or at wire speed, as claimed. The pipeline processor of Gentieu merely generates data for high speed serial data protocols (col. 2, lns 51-53).

Hipp discloses a client server computer network having virtual port multiplexing where communications between client computers and application servers that are intended for a physical port are multiplexed and rerouted to alternative ports to allow a plurality of client computers and applications to send and receive data at the same port number (see [0002]). As described in paragraph [0025], Hipp's virtual port multiplexer (VPM) manages connection requests from applications. When an application attempts to connect to another application through a port on which a connection already exists, the VPM creates a new virtual port to provide a separate communication path between the applications and redirects (multiplexes) the second connection request through the newly created virtual port to allow simultaneous access while avoiding interference. This is not the same as translating a virtual storage target address in a received data packet to a physical storage target address, as claimed.

Moreover, Gentieu's pipeline processor does not route data packets between servers and physical storage targets, as claimed, nor without buffering. It is respectfully pointed out to the Examiner that it is impermissible to speculate that Hipp

converts between port addresses without buffering because Hipp is silent about buffering, and that is improper to base a rejection on the absence of an explicit disclosure of no buffering.

Additionally, Gentieu and Hipp are directed to quite different and unrelated areas of technology, and the references cannot be combined as done by the Office. Nothing in Gentieu or Hipp teaches or suggests combining Gentieu's processor for converting data protocols with Hipp's virtual port multiplexing in a client application server network, and it is respectfully submitted that the teachings of these references are not enabling for the combination proposed by the Office, and that the references cannot be combined to afford packet address virtualization, as claimed.

Converting data protocols using a pipeline processor, as done by Gentieu, is substantially different from and unrelated to creating virtual ports for avoiding interference between two or more clients attempting to access the same physical port, as taught by Hipp. It is not clear how the two references could even be combined, as suggested by the Office, or how a synchronous pipeline processor that operates on serial data could even be adapted to monitor application requests and create new virtual ports, as done by Hipp.

The references are incompatible and cannot be combined as proposed by the Office. The Office has failed to make out a *prima facie* case to support its rejection by failing to demonstrate how one skilled in the art could make the proposed combination and produce the claimed invention, or if they did, how the combination of a protocol processor and a virtual port address module would produce the claimed invention. It is

respectfully pointed out to the Office that the references in combination must render the invention considered as a whole obvious to one skilled in the art, not simply that elements disclosed by the references be selectively chosen and combined without regard to their disclosed purpose, function or compatibility.

As pointed out by the Supreme Court in *KSR v. Teleflex*, 550 U.S. 398, 82 USPQ 2d 1385 (2007), obviousness cannot be proved by merely demonstrating that each of the elements of the invention was independently known in the prior art. Rather, to show obviousness, the elements must be capable of being combined without changes in their respective functions, and the combinations would have yielded predictable results to one skilled in the art at the time of the invention. Here, the elements of Gentieu and Hipp could not have been combined with no change in their respective functions and predictably yielded the claimed invention.

As to the Office's statement that it would have been obvious to modify the processor of Gentieu to include a multiplexer as disclosed by Hipp, it is respectfully pointed out to the Office that the function of Hipp's multiplexer is substantially different from the claimed translation of virtual addresses to physical addresses, and the proposed modification of Gentieu's processor to incorporate the function of Hipp's multiplexer would require changing the structure, function and operation of the processor and multiplexer in ways that are nowhere taught by the references and that would not be not apparent to one skilled in the art. Any such modifications would amount to substantial reconstruction of both the processor and the multiplexer. Thus, such proposed modification is purely unsupportable speculation.

The foregoing discussion and principles concerning combinations of references for obviousness rejections are applicable to all of the present rejections under 35 U.S.C. §103, and are incorporated by reference into the following arguments.

Contrary to the Office's assertion, the communication device of Gentieu is not equivalent to a storage switch that routes packets between a server and a physical storage device by translating virtual storage target addresses to physical storage target addresses, as claimed. It is respectfully pointed out that the disclosed protocol conversion communications device of the Gentieu does not route data packets between a server and a storage device, and is not equivalent to a storage switch as claimed.

Accordingly, it is respectfully submitted that Gentieu and Hipp references cannot render independent Claims 1 and 9, or dependent Claims 2-8 obvious.

Claims 3-8, 10-13, 34, 35, 24-26 and 29-33

The rejections of Claims 3-8, 10-13, 34, 35, 24-26 and 29-33 comprising independent Claims 10, 12, 24, 29, 30, 31, 32 and 34 as unpatentable over Gentieu, Hipp and further in view of Morgan are traversed.

Independent Claims 10, 12 and 14 are method claims, and Claim 34 is directed to a program executable by a processor to perform a method. These claims recite, in somewhat different ways, translating a virtual storage target address in a packet to a physical storage target address without either buffering the packet or at wire speed, in a manner similar to Claims 1 and 9, and these claims distinguish over Gentieu and Hipp for the reasons pointed out above that Claims 1 and 9 distinguish. The claims

also call for the ports that receive a packet or that communicate with a target to be on linecards.

Morgan discloses nothing more than linecards having ports that are connected to and communicate with a computer backplane bus. Morgan has little to the teachings of Gentieu and Hipp, does not cure the deficiencies in the teachings of these references.

Accordingly, Claims 10, 12, 14 and 34, and the claims depending therefrom, are deemed allowable over Gentieu, Hipp and Morgan for the same reasons discussed above in connection with Independent Claims 1 and 9.

Claim 24

Independent Claim 24 is directed to a storage switch having a processor unit that performs a virtualization function to translate a virtual target address of a virtual storage target provisioned on a physical storage target to a physical storage target address of the physical storage target without buffering the packet, and includes a CPU in communication with the processor unit which sends a virtual target descriptor with information to the processor to operate on data for the virtual storage target.

None of the references to Gentieu, Hipp or Morgan discloses or suggests a storage switch, as claimed, which includes a CPU in communication with a processor unit that communicates with a port receiving a packet to perform a virtualization function, where the CPU sends the processing unit a virtual target descriptor having information to operate on data for the virtual storage target. Accordingly, these references cannot render Claim 24 are the claims dependent thereon obvious.

Claim 29

Independent Claim 29 is directed to a storage switch for routing packets between servers and physical storage targets. The switch includes a plurality of ports on respective linecards, each having a processor unit for receiving a packet destined for a virtual target and including a virtualization unit for translating at wire speed an address in the packet from a virtual target address to a physical target address.

The cited references do not teach or suggest a storage switch for virtual to physical address translation, as claimed.

Claims 30 and 32

Independent Claim 30 calls for a linecard of a storage switch having means for performing a virtualization function by translating a virtual target address of a virtual storage target provisioned on a physical storage target connected to the port to a physical target address of the physical storage target , without buffering the packet, as claimed.

Independent Claim 32 is directed to a storage switch having linecards, and is similar to Claim 30 in calling for means for translating a virtual target address of a virtual storage target provisioned on a physical storage target connected to a port of the linecard to a physical target address of a physical storage target to a physical target address.

These means plus function elements of Claims 30 and 32 must be interpreted pursuant to 35 U.S.C. §112, ¶6 as corresponding to the structure, material and acts disclosed in specification for performing the recited function, and equivalents thereof.

The Office Action fails to point to structure, materials or acts in the cited references corresponding to structure, materials or acts disclosed in the specification, or equivalent thereto, for performing the recited functions in these two claims. Thus, the Office has failed to satisfy its burden of establishing a *prima facie* rejection, and the rejections are improper for this reason alone.

Moreover, for the reasons already pointed out above, the references do not disclose or suggest virtualizing packets, as claimed, and also cannot render Claims 30 and 32 obvious and unpatentable for these reasons.

Claim 31

Independent Claim 31, which is somewhat similar to Claim 24, calls for a linecard of a storage switch having a plurality of ports with corresponding plurality of processors in which each processor includes "a wire-speed virtualization unit that translates a virtual target address of a virtual storage target to a physical target address of a physical storage target on which said virtual storage target is provisioned", stored virtual target descriptors and physical target descriptors, and a CPU in communication with the processor. There is no teaching or suggestion in the references of a linecard having a plurality of ports and processor units that communicate with a CPU, as set forth in Claim 31. Accordingly, it is submitted the references cannot render this claim obvious and unpatentable.

Claim 34

Claim 34 is directed to a set of software instructions executable by a processor for performing a method substantially corresponding to the method as set forth in

Claim 10, and Claim 34 is deemed to be allowable over the cited references for the same reasons Claim 10 is deemed to be allowable.

Claims 14, 15 and 18

The rejection of Independent Claim 14, and Claims 15 and 18 as unpatentable over Tzeng in view of Latif is respectfully traversed.

Claim 14 has been amended similarly to other independent method Claims 1, 9, 10 and 12 to set forth that it is directed to a method by a storage switch for routing packets between servers and physical storage targets. As set forth in Claim 14, an ingress linecard receiving a packet retrieves information about a virtual storage target from a virtual target descriptor that includes a flow ID for routing the packet through the switch. The ingress linecard places a virtual target descriptor identifier and the flow ID in a local header of the packet, and forwards the packet to an egress linecard in accordance with the flow ID. The egress linecard uses the virtual target descriptor identifier to identify a physical storage target on which the virtual storage target is provisioned, and to convert a virtual target block address of the virtual storage target to a physical target block address of the identified physical storage target, without buffering the packet, and sends the packet to the physical storage target.

Tzeng discloses a layer 2 switch where incoming packets are identified as to format type. However, Tzeng stores data frames in a buffer memory 28 while processing the packets to make forwarding decisions. (see col. 3, lns. 51 – 67 and Fig. 1). While Tzeng may teach buffer-free identification, the reference explicitly teaches buffering for processing packets for forwarding.

The Latif patent teaches a network switch for transferring data between network devices which operate using different data protocols, where input protocols are converted to an internal data format, processed, and then reconverted to an output protocol. Latiff does not teach or suggest, as required by Claim 14:

- retrieving by an ingress linecard a virtual target descriptor and information, including a flowID for a received packet,

- routing the packet through the switch using the flowID to an egress linecard, and the egress line card using the information about the physical storage target to convert a virtual target block address to a physical target block address, without buffering the packet, or

- sending the packet to the physical storage target using the physical target block address.

Rather, Latiff in Figures 6a-c (referred to by the Examiner) and at col. 8, ln.10 - col. 9, ln. 46 teaches encapsulation of Fibre Channel (FC) packets in an Ethernet frame for transfer over an IP network, since FCP frames are incompatible with Ethernet interfaces. Encapsulation of an entire packet is not the same as the claimed placing of a flowID and a virtual target descriptor in a local header of a packet, as asserted by the Office.

Both Tzeng and Latiff (see col. 15, lns. 14-17) explicitly teach buffering, and, accordingly, do not teach or suggest the packet virtualizing method as recited in Claim 14. Accordingly, the references cannot render Clam 14 or the claims dependent thereon unpatentable.

It is respectfully submitted that the cited prior art cannot be combined in the ways suggested by the Office, and that this prior art does not teach or suggest a method for use in a storage switch, a storage switch, a linecard for a storage switch, or a method preformed by a processor in a storage switch executing software instructions, as set forth in Claims 1-16, 18 and 24-35. Accordingly, this prior art cannot render the claims obvious and unpatentable.

In view of the foregoing, it is respectfully submitted that all rejections have been overcome and that this application is in condition for allowance. Accordingly, favorable reconsideration of this application is requested, and early allowance of all claims is solicited.

The specification has been amended to update the status of the referenced applications on page 1.

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Respectfully Submitted,

/Barry N, Young/

Barry N. Young
Attorney for Assignee
Reg. No. 27,744

Customer No. 80280
Law Offices of Barry N. Young
200 Page Mill Road, Suite 102
Palo Alto, CA 94306-2061
Phone: (650) 326-2701
Fax: (650) 326-2799
byoung@young-iplaw.com